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(71) Applicant *(for all designated States except US)*: TELEFONAKTIEBOLAGET LM ERICSSON (publ) [SE/SE]; S-164 83 Stockholm (SE).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: GEVORGIAN, Spartak [AM/SE]; Adler Salvius gata 15, S-411 11 Göteborg (SE). JACOBSSON, Harald [SE/SE]; Fullriggaregatan 10A, S-426 74 Västra Frölunda (SE). LEWIN, Thomas [SE/SE]; Landstormsvägen 40, S-439 94 onsala (SE).

(74) Agent: ALBIHNS GÖTEBORG AB; Box 142, S-401 22 Göteborg (SE).

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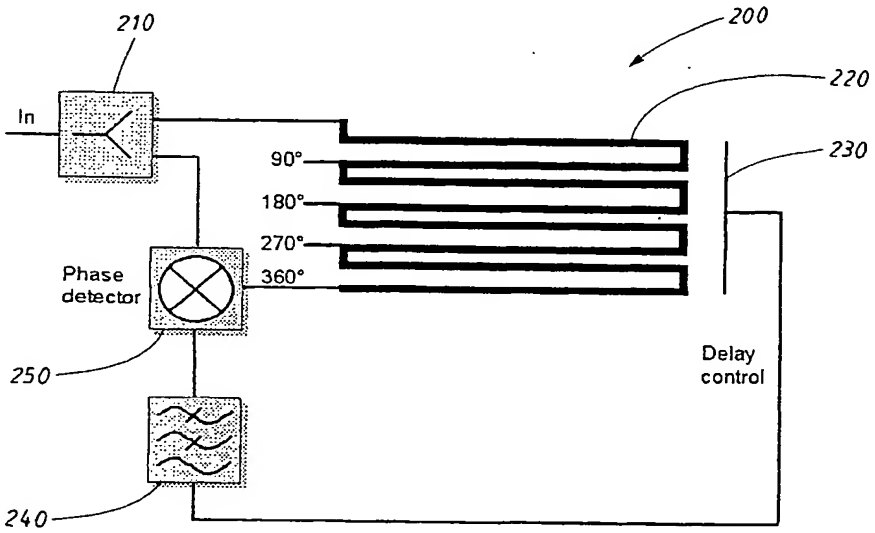
(54) Title: A DELAY-LOCKED LOOP WITH PRECISION CONTROLLED DELAY



(57) Abstract: The invention discloses a delay-locked loop circuit (200) with input means (210) for a signal that is to be delayed, the input means comprising means for splitting the input signal into a first and a second branch. The signal in the first branch is connected to a component (220) for delaying the signal, and the signal in the second branch is used as a non-delayed reference for the delay caused by the delay component in the first branch. The delay component (220) is a passive tunable delay line, and the circuit comprises tuning means (230) for the tunable delay line, the tuning means being affected by said reference signal, and the first branch comprises output means for outputting a delayed signal with a chosen phase delay. Suitably, the delay component (220) is continuously tunable, for example a tunable ferroelectric delay line.

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